<u>REMARKS/ARGUMENTS</u>

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-8 and 11-14 are presently active in this case, Claim 1 having been amended to include the features of Claims 9-10, Claims 11-14 having been amended to depend from amended Claim 1, and Claims 9-10 and 15-20 having been canceled by the present amendment. No new matter has been added.

In the outstanding Office Action, Claims 1-6 were rejected under 35 USC §102(b) as anticipated by <u>Zulian et al.</u> (USP 5,701,413, hereinafter "<u>Zulian</u>"); Claims 7-8 were rejected under 35 USC §103(a) as being unpatentable over <u>Zulian</u> in view of <u>Cohen</u> (USP 6,026,464); Claims 9, 10, 15 and 16 were rejected under 35 USC §103(a) as being unpatentable over <u>Zulian</u> in view of <u>Waldecker et al.</u> (USP 4,669,056); and Claims 11-14 and 17-20 were rejected under 35 USC §103(a) as being unpatentable over <u>Zulian et al.</u> in view of <u>Waldecker et al.</u> and <u>Cohen</u>.

In light of the outstanding grounds for rejection, Claim 1 has been amended to include the subject matter of original Claims 9 and 10, which have been canceled. In view of the amendment to Claim 1, amended Claim 1 is believed to be clearly patentably distinguishing over the cited prior art, for the reasons next discussed.

As is evident from amended Claim 1, the present invention utilizes the creation and application of transfer directives to establish and control communication of data. Accordingly, Claim 1 recites, in part, a transfer controller that sends a transfer directive to the network and memories. The network transfers data based on the transfer directive at a predetermined timing. Also the memories receive and store data from the network based on the transfer directive. In the disclosed embodiment, for example, the transfer controller 203 receives a data transfer request from a prescribed requester and proceeds to secure a network

connection to the network 201, conduct macro access arbitration such that the memory

module to be accessed is used effectively, and secure authorization to access the macro.

Then, in consideration of the transfer timing, the transfer controller 203 directs the requester

to transfer the data, sends switching information to the network, and sends a command to the

memory module. That is to say, the transfer controller controls data transfer timing for the

memories, the network and the requester by using the transfer directive. Zulian neither

discloses the concept of transfer directives, or their use, or their functionality.

Furthermore, amended Claim 1 recites a module arbitration unit which also is not is

evident in Zulian. Instead, in Fig. 3 of Zulian, a system controller 15, which is believed to

correspond to the transfer controller recited in Claim 1, has a logic 70 for arbitrating access to

the system bus. The logic 70 receives access requests from processors and grants access to

the system bus by sending a response signal ABGRANT(i) on one of a plurality of point to

point connections with the various processors. In contrast, according to the claimed

invention, there is provided a module arbitration unit that includes module arbiters that hold

the transfer request and arbitrates transfer requests for each module. By performing

arbitration of the network and arbitration of the memory modules taking into account the

control of the macros of the memory modules, the claimed invention makes it possible to

perform scheduling at the cycle level, by which it is possible to reduce or even eliminate the

need for a large-capacity intermediate buffer. Furthermore, by performing network

arbitration in synchronization with the access timing of the memory modules, the network

resources can be used effectively without occupying the network continuously in the

conventional manner.

Further, it is respectfully submitted that the cited secondary references do not curer

the deficiencies of the Zulian reference above discussed. The outstanding Office Action

relies on Cohen as teaching a data transfer system as claimed in claim 1, wherein the plurality

of modules includes a plurality of macros the data is divided to be stored by the plurality of macros. It is the Applicants' view, however, that <u>Cohen</u>, like <u>Zulian</u>, does not disclose the module arbitration unit as recited in Claim 1.

The outstanding Office Action finds that <u>Waldecker</u> disclose a module arbitration unit. <u>Waldecker</u> in its abstract notes, "[o]ne or more of the processors have means for monitoring the bus in order to determine whether an address on the bus has been transferred to the first or the second storage unit during a particular transfer interval." Thus according to <u>Waldecker</u> the bus is monitored to determine if an address on the bus is transferred to the first or second storage unit. Contrary to this, the module arbitration unit as recited in Claim 1 arbitrates of decoded data transfer requests on a per-module basis. That is to say, the claimed module arbitration unit arbitrates a data transfer request, whereas <u>Waldecker's</u> "means for monitoring" determines where the address is transferred. In view of this distinction, it is respectfully submitted that <u>Waldecker</u> does not cure the deficiencies of <u>Zulian</u> and <u>Cohen</u> and that the amended claims patentably distinguish over the cited references.

Consequently, in view of the present amendment and in light of the above comments, no further issues are outstanding, and the amended claims are believed to be allowable. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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